REMARKS

I. Status of the Application

Claims 24 and 26-39 are pending in this application. In the July 18, 2008 office action, the Examiner:

A. Rejected claim 30 under 35 U.S.C. § 112 for not particularly pointing out and distinctly claiming the subject matter which the applicant regards as the invention;

B. Rejected claims 24, 26-34 and 37-39 under 35 U.S.C. §103(a) as allegedly being unpatentable over US 5,917,355 to Klass in view of applicant's admitted prior art; and

C. Rejected claims 35 and 36 under 35 U.S.C. §103(a) as being unpatentable over Klass.

In this response, applicants have amended claim 30. The examiner's rejections of claims 24 and 26-39 are respectfully traversed in view of the foregoing comments and the following remarks.

II. The Rejection of Claim 30 Under 35 U.S.C. § 112 Should be Withdrawn

In the July 18, 2008 Office action, the examiner rejected claim 30 under 35 U.S.C. § 112 for not particularly pointing out and distinctly claiming the subject matter which the applicant regards as the invention. Claim 30 has been amended in this response to correct a clerical error in the claim as originally filed. In view of the amendment to claim 30, it is respectfully submitted that the examiner's rejection of claim 30 under 35 U.S.C. § 112 is now moot and should be withdrawn.

III. The Rejection of Independent Claims 27, 35 and 36 Should be Withdrawn

In the July 18, 2008 office action, the Examiner rejected claims 27, 35 and 36 under 35 U.S.C. § 103(a) as being unpatentable over Klass in view of applicant's admitted prior art (AAPA). In this response, Applicant respectfully traverses the Examiner's rejection of claim 27 under 35 U.S.C. § 103(a).

The Examiner's rationale for a finding of obviousness in the July 18, 2008 Office action is not specifically stated in the context of the examples of MPEP § 2143. However, Applicant notes that pursuant to MPEP 2143, "the key to supporting any rejection under 35 U.S.C. § 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." Furthermore, in order to establish a *prima facie* case of obviousness, three basic criteria should be met as set forth in MPEP § 2143.01-2143.03. First, all claim limitations must be considered. MPEP § 2143.03. Second, there must be some suggestion or motivation to modify the references or combine reference teachings. MPEP § 2143.01. Third, there must be a reasonable expectation of success. MPEP § 2143.02.

As set forth in the following paragraphs, it is respectfully submitted that the examiner has failed to make a prima facie case of obviousness with respect to claim 27 since, (i) all claim limitations are not shown in the cited references, (ii) there is no motivation to combine the references as argued by the examiner, and (iii) there is no reasonable expectation for success. Claims 35 and 36 include several similar limitations as those found claim 27, and several of the arguments set forth below also apply to independent claims 35 and 36.

A. "A Programmable Capacitor Unit"

In the July 18, 2008 Office action, the examiner admitted that Klass fails to teach a "programmable capacitor unit" (see paragraph 7, line 4 at page 3 of the July 18, 2008 Office action). However, neither Klass nor AAPA refers to a "*programmable* capacitor". As set forth in the present application, implementation of the programmable capacitor unit permits the programming of a time constant for charging and discharging of the circuit node. Accordingly, claim 27 clearly calls for a "programmable capacitor unit arranged to charge ... and to discharge". Again, neither Klass nor AAPA refers to such a programmable capacitor unit, and the examiner did not even attempt to argue that programmable capacitor unit is taught or suggested by Klass or AAPA. Accordingly, because all the claim limitations are not shown, the examiner has failed to make a prima facie case of obviousness, and the examiner's rejection of claim 27 under 35 U.S.C. § 103(a) should be withdrawn for at least this reason.

B. The "Programmable Capacitor Unit Coupling a Circuit Node to a Reference Potential"

In the July 18, 2008 Office action, the examiner admitted that Klass fails to teach a "programmable capacitor unit coupling a circuit node to a reference potential". The examiner then took official notice that "it is notoriously old and well known that a capacitor connected to ground at an output to any circuit serves as a filter" and concluded that "it would have been obvious to one of ordinary skill in the art ... to include a capacitor directly connected between ground and node X of Klass's invention in order to filter noise" (see paragraph 7, lines 5-9 of the July 18, 2008 Office action).

Applicant respectfully traverses the examiner's suggestion that connecting a capacitor to an output node of a signal level displacement would be generally accepted as an obvious measure used to filter noise. There is no reason to filter noise in connection with a signal level displacement circuit for a flip flop, and the examiner has not suggested a reason for doing so. Even if one were to assume that a person skilled in the art would use a capacitor connected to ground as a filter, there is no reason to combine the concept of a noise filter with a signal level displacement circuit for a flip flop or prior art suggested by the examiner including Klass. Thus, (i) the limitation of "a programmable capacitor unit coupling a circuit node [of a signal level displacement circuit for a flip flop] to a reference potential" is not shown in the cited references, (ii) there is no motivation to modify the Klass reference as argued by the examiner, and (iii) there would be no reasonable expectation for success with such a modification. Accordingly, it is respectfully submitted that the examiner has failed to make a prima facie case of obviousness, and the examiner's rejection of claim 27 under 35 U.S.C. § 103(a) should be withdrawn for at least this reason.

C. "A First Isolating Circuit ... And ... A Second Isolating Circuit"

In the July 18, 2008 Office Action, the examiner argued that the slave latch (303) shown in Fig. 4 of Klass could be modified to be included with the transmission gate (TG) and the slave latch as shown in AAPA (figure 4 of the present application) to arrive at the limitation of "a first isolating circuit configured to be clocked by the clock signal and having an input connected to the circuit node; a second isolating circuit configured and arranged to be clocked by the delayed clock signal; wherein an output of the first isolating circuit feeds back to the input of the first isolating circuit via the second isolating circuit" (see paragraph 7, pages

3-4 of the July 18, 2008 Office action). Applicant respectfully traverses the examiner's argument.

As disclosed in figure 13 of the present application, the first isolating circuit node denoted 12 may comprise an inverter stage with a transmission gate connected downstream wherein the transmission gate is clocked by the clock signal CLK. The second isolating circuit 29 can comprise an inverter and a transmission gate connected downstream which is clocked by the delayed clock signal CLK_{delay}. The prior art configuration as shown in figure 4 of the present application does not disclose the limitation of claim 27 of a first isolating circuit configured to be clocked by a *clock* signal and a second isolating circuit configured to be clocked by the *delayed clock* signal. By contrast, the prior art of figure 4 shows a transmission gate clocked by a CLK and a latch circuit wherein one individual inverter is clocked by the inverted clock signal CLK. Substituting Klass's slave latch 303 with the slave latch and transmission gate of figure 4 of the present application does not yield any predictable result, and cannot be considered equivalent to the limitations of claim 1 with respect to the first and second isolating circuit. Furthermore, there is no disclosure in Klass that the second isolating circuit should be clocked by the delayed clock signal.

D. "Delayed and Inverted Clock Signal"

In the July 18, 2008 Office action, the examiner argued with that the circuit node (X) in figure 4 of Klass is "arranged to charge a capacitor (C) in a charging phase in response to the clock signal being logically low and to discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and a delayed clock signal being logically high" (see paragraph 7 of the July 18, 2008 Office action). However, this is not what

is called for in pending claim 27. Instead, pending claim 27 calls for "a programmable capacitor unit ... arranged to ... discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and the *delayed and inverted* clock signal being logically high" (emphasis added). Therefore, Klass does not disclose this limitation of claim 27 as argued by the examiner. Furthermore, input stage 301 as shown in figure 4 of Klass cannot be used as a signal level displacement circuit for a flip flop.

Even assuming *arguendo* that the input stage 301 shown in Fig. 4 of Klass could be used as a "signal level displacement circuit", the evaluation phase according to Klass functions differently than what is set forth in claim 27. In particular, Klass does not teach or suggest the generation of a "delayed and inverted clock signal". Instead, at column 5, lines 56-62 of Klass, it is disclosed that the flip flop circuit of figure 4 operates in an evaluation phase when the clock signal CK is at a logical high level. Klass further teaches that the inverters INV1 and INV2 delay the clock signal CK to generate a delayed clock signal CKD (see column 6, lines 37-41 of Klass). Thus, a person skilled in the art would read the combination of inverters INV1 and INV as a delay element, such as that shown as reference numeral 13a in figure 13 of the present application. There is simply no teaching in Klass of the generation of a delayed and inverted clock signal. The timing diagrams of figures 5 and 6 in Klass show that during the time period where CK is logic high level and a potentially inverted CKD has a logic high level, the potential at node X (see curves 509 and 609) always remains at a logic high level with respect to the logic state of the data input D (see curves 505 and 605). This is because Klass teaches the use of a static latch formed by inverters INV3 and INV4 being coupled to node X. Thus, operating input stage 301 of Klass where the clock signal CK has a logic high level

results in PMOS transistor P1 being off, NMOS transistor N3 being on, and the delayed clock signal CKD acquiring a logic high level after a time delay, which adjusted as taught in column 6, lines 49 and 43, i.e., the low-to-high transition of the delayed clock signal CKD occurs slightly after a high-to-low transition of the internal signal at node X.

The above-described operation node results in a circuit diagram the same as that attached hereto as Exhibit A. In the attached figure off and on transistors are omitted. In contrast to the signal level displacement circuit of claim 27 wherein a programmable capacitor unit is arranged to discharge "depending on a data signal in response to the clock signal being logically high and the delayed and inverted clock signal being logically high", Klass does not teach any comparison of a clock signal CK and a delayed clock signal CKD or between a clock signal CK and an inverted and delayed clock signal. While according to the present application this charging occurs as a function of a data signal, a clock signal and a delayed and inverted clock signal, the teaching of Klass relies on the logic level at node X in a preceding clock cycle which is reflected by a stable latch circuit formed by INV4 and INV3.

As set forth above, Klass does not teach the limitation of claim 27 of "a programmable capacitor unit arranged to ... discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and the delayed and inverted clock signal being logically high". There is also no suggestion or motivation in Klass or in AAPA to provide such limitation. Therefore, the examiner has not made a prima facie case of obviousness with respect to claim 27, and the examiner's rejection of claim 27 under 35 U.S.C. § 103(a) should be withdrawn.

IV. The Rejection of Dependent Claims 24, 26-34 and 37-39 Should be Withdrawn

Dependent claims 24, 26-34 and 37-39 all depend from and incorporate all the limitations of independent claim 27. Moreover, each of these dependent claims includes additional novel and non-obvious limitations. Accordingly, it is respectfully submitted that dependent claims 24, 26-34 and 37-39 are also allowable for at least the same reasons that independent claim 27 is allowable, as well as additional reasons. Therefore, the examiner's rejection of claims 24, 26-34 and 37-39 should be withdrawn.

One example of a limitation of a dependent claim not found in the cited references is the limitation of claim 24 of "the circuit node is arranged to discharge in the evaluation phase in response to the data signal being logically high and the circuit node is arranged to not discharge in the evaluation phase in response to the data signal being logically low". In the July 18, 2008 Office action, the examiner argued that it would be inherent based upon the structure disclosed in Klass that charging occurs when the data signal is logically high and no discharge occurs when the data signal is low. However, it should be noted that no capacitor is coupled to the node X in Klass. Thus, in principle no charging can be induced, however a static latch formed by inverters INV3 and INV4 is provided. Therefore, charging and discharging according to Klass is dependent on a stored logic level by the static latch and the stray capacitance of this latch. Accordingly, for at least this reason, the examiner's rejection of claim 24 under 35 U.S.C. § 103(a) should be withdrawn.

With respect to claim 26, as elaborated above, neither figure 4 of the present application nor Klass discloses isolating circuits clocked by differently delayed clock signals. Rather, Klass teaches the use of a static latch of inverters (INV3 and INV4) to buffer-store the

logic level present on node X. Accordingly, for at least this reason, the examiner's rejection of claim 26 under 35 U.S.C. § 103(a) should be withdrawn.

With respect to claim 28, is should be noted that neither Klass, figure 4 of the present application, nor the examiner's alleged inherency in the combination of Klass and AAPA teaches the limitation of "wherein the signal delay circuit, the circuit node, and the programmable capacitor network are incorporated into a master latch circuit". As set forth in MPEP ()S 221, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." The examiner made no such showing in the July 18, 2008 Office action that the limitation of claim 28 is inherently disclosed in Klass and AAPA. Accordingly, for at least this reason, the examiner's rejection of claim 28 under 35 U.S.C. § 103(a) should be withdrawn.

With respect to claim 29, the examiner reads the PMOS transistor P1 and input lead 307 in figure 4 of Klass as disclosing the limitation of "the master latch circuit ... include[ing] an inverter configured to generate an inverted clock signal corresponding to an inversion of the clock signal". However, identifying P1 as an inverter results in having the clock signal CK permanently coupled to the circuit node X. Further, an inverter usually comprises at least two complementary transistors. Therefore, the examiner has not made a prima facie case that the limitations of claim 29 are disclosed in the combination of Klass and AAPA, and the examiner's rejection of claim 29 should be withdrawn.

With respect to claim 31, none of the MOS transistors P1 or N1-N4 of Klass are controlled as a function of a delayed and inverted clock signal. Specifically, Klass does not

disclose the limitation of "the master latch circuit is configured to generate a delayed inverted clock signal and to drive the second controllable switch with the *delayed inverted clock signal*" (emphasis added). Accordingly, it is respectfully submitted that the combination of Klass and AAPA does not disclose all the limitations of claims 30 and 31, and for at least this reason, the examiner's rejection of claim 31 should be withdrawn.

V. Conclusion

For all of the foregoing reasons, it is respectfully submitted the applicant has made a patentable contribution to the art. Favorable reconsideration and allowance of this application is therefore respectfully requested.

Because the deadline for responding to the July 18, 2008 Office action fell on Saturday, October 18, 2008, this response is being timely filed on Monday, October 20, 2008. In the event applicant has inadvertently overlooked the need for an extension of time or payment of an additional fee, the applicant conditionally petitions therefore, and authorizes any fee deficiency to be charged to deposit account 13-0014.

Respectfully submitted,

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